GATE MODULATION FOR HIGH POWER AMPLIFIERS

Field of the Invention

The present invention relates to high power amplifiers, and in particular to gate modulation of high power amplifiers for efficient operation.

Background of the Invention

Telecommunications base stations use ultra linear radio frequency (RF) high power amplifiers for transmitting signals to remote communication devices such as cellular telephones. The amplifiers use transistors to amplify RF signals for transmission. The requirement of ultra high linearity dictates that the transistors be biased electrically in such a way that minimal distortion is imposed upon the amplified signal. Unfortunately, such biasing results in the transistor(s) requiring continuous electrical power, even when the magnitude of the signal to be amplified is zero.

Current high power amplifier designs for use in Code Division Multiple Access (CDMA) base stations have an efficiency of approximately 13% when operating at maximum rated output power. This low efficiency results in the need to disperse heat generated by the excess power consumed. It also results in base station packaging being physically large, complex and costly.

There is a need to reduce the power consumption of high power amplifiers without affecting the linearity of the amplification. There is a further need to reduce the need for large, complex and costly packaging for RF high power amplifiers caused by excess heat generation.

Summary of the Invention

A high power RF amplifier utilizes dynamic biasing for transistors in an output stage of the amplifier. In one embodiment, as the magnitude of an RF signal to be amplified falls below a predetermined level, the biasing signal is turned off to reduce power consumption. A gate bias voltage is used to switch the transistors off and on. A low pass filter is employed to eliminate noise generated at the output of the amplifier caused by the instantaneous switching, while not impacting the amplifier's response to low-high magnitude transients.

In a further embodiment, I and Q data from baseband digital data is sampled and buffered prior to being transformed and provided to a RF power amplifier. A gate bias signal is controlled based on current samples in order to control the power amplifier in a manner appropriate for the current samples when provided from the buffer. If the current sample and next samples are less than a threshold, the gate bias is removed. If the current sample and next samples are greater than the threshold, the gate bias is present.

Brief Description of the Drawings

Figure 1 is a block diagram of dynamic biased transistors in the output stages of an RF power amplifier in accordance with the present invention.

Figure 2 is a block diagram of a further embodiment of the RF power amplifier of Figure 1.

Detailed Description of the Invention

A radio frequency (RF) power amplifier is indicated generally at 100 in Figure 1. A diode detector 110 samples the envelope of a Code Division Multiple Access (CDMA) input waveform 115. The diode detector 110 converts the RF signal into a voltage which is a function of the magnitude of the envelope of the RF signal. It produces a voltage that is related to the magnitude of the envelope of the RF input signal 115. An RF coupler 117 is coupled between the RF input 115 and the diode detector circuit 110 to provide a relatively non-invasive means of sampling the voltage of the input signal.

The output of the diode detector 110 is coupled to a comparator 120, which switches a gate bias control FET 130 which is biased by a gate bias voltage circuit 135. The comparator 120 compares the output of the diode detector circuit with a threshold voltage level. If the output of the diode detector falls below the threshold voltage, then the output of the comparator changes state, either from low-to-high, or high-to-low, in different embodiments.

FET 130 provides a switched path for the gate bias supply voltage provided by circuit 135. Normally, a gate bias supply voltage is optimized for a particular application referred to as setting the operating point of the transistors. Changes in the gate bias level typically cause changes in gain, linearity, and quiescent DC current, and ultimately the temperature of the function, which in turn affects gain and

linearity. It is desirable to keep the gate bias voltages relatively static. In some applications, a small change in gate bias over temperature may be required to compensate for temperature effects. Gate bias circuit 135 in one embodiment is a regulated DC supply that provides a low-noise voltage source. It comprises an integrated voltage regulator, a potentiometer for precise trimming of the voltage, and a selection of capacitors for filtering.

The gate terminal of the FET is coupled to the comparator circuit 120, the drain terminal of the FET is coupled to the gate bias voltage circuit, and the source terminal of the FET is coupled to the low pass filter 140. In this embodiment, when the FET 130 is switched on by the comparator, a low impedance path is formed between its drain and source terminals. When the FET 130 is switched off, a high impedance path exists. The potential different between the gate and source terminals of the FET determine the impedance between its source and drain terminals.

A low pass filter 140 is coupled to the output of the FET 130 to avoid unwanted spurious emissions caused by sudden switching of the gate of the FET 130. Low pass filter 140 attenuates high frequency components of the gate bias voltage signal, which is switched by the FET. When the FET switches on or off, the gate bias voltage signal is essentially a step function, which has some energy at all frequencies. Therefore, a low pass filter, such as an R-C network, ensures that any high frequency components generated by the switching are attenuated sufficiently, before being delivered to the gates of output power transistors 150. The output power transistors 150 provide an RF output 155.

In one embodiment, the threshold voltage is set using empirical test data. It is difficult to reliably predict or to have knowledge of the (envelope of the) RF signal, which is about to be delivered to the amplifier. Therefore, the threshold voltage is set conservatively, and some hysteresis is employed to ensure that the gate bias is always restored when the magnitude of the envelope of the RF input signal exceeds a certain value.

In a further embodiment shown in Figure 2, a "digital baseband in" system is shown generally at 200. A gate switching system 210 generates a Gate bias switching signal by sampling digital baseband I and Q data, and provides it to gates of an RF power amplifier 220 via line 225.

I and Q data is streamed from the output of a Tx ASIC 230, together with a Tx clock which is normally used to clock Tx DACs inside an upconverter. The I and Q

data is fed through two separate FIFO buffers 235 and 240, which act as digital delays to a baseband to RF up-converter 243 which provides RF signals to the RF power amplifier 220. Both FIFO buffers hold D samples.

Prior to these two FIFO buffers, I and Q digital baseband data is converted into a digital representation of RF power, by applying a formula such as $P= |(I^2+Q^2)|$ at 245 in gate switching system 210. The continuous stream of P values are fed into a P FIFO buffer 250, also of length D samples, which offers non-invasive, parallel access. The P FIFO buffer 250 therefore contains a representation of RF power vs. time. A minimum value of M must be predetermined for the particular application by consideration at least the following factors; the time constant of low pass filter 140, τ, the rate at which baseband data is processed, F_s.

In general, a value of M should be chosen such that $M > 2 \tau F_s$, thus ensuring that low pass filter 140 may discharge and recharge significantly during the time period that the gate bias switching signal 225 is a logic low. The value of D in one embodiment is greater than or equal to M.

The last M values of the P FIFO buffer 250 are sampled, and if they are all less than a Pthreshold value, P_{thresh}, which is a digital representation of RF power derived from the I and Q baseband signals, then, as determined at comparator logic 255, a logic low is generated, otherwise a logic high is generated. This logic signal is fed to the Gate bias switch control input of the RF Power Amplifier 220. The Gate bias switching signal will be zero, and therefore the Gate bias of the RF power amplifier will be removed if; the current sample and next (M-1) samples of P are less than P_{thresh}. The Gate bias switching signal will be one, and therefore the Gate bias of the RF power amplifier will be present if; either the current sample, or any of the next (M-1) samples of P are greater than or equal to P_{thresh}. P_{thresh} is determined empirically in one embodiment to obtain a desired tradeoff between power conservation and performance. In further embodiments, P_{thresh} is set such that a maximum amount of power is conserved without degradation of performance.

The invention can be used for any amplifier application where the modulation scheme dictates that the magnitude of the envelope of the RF signal regularly approaches zero. Regardless of the modulation scheme, a high power linear amplifier consumes considerably less power in cases where the RF input signal is removed. The thresholds for turning the power amplifier on and off are approximate, and may

be used in a manner such that switching occurs when the signal being compared is equal to, less than, or greater than as desired.